IN THE ABSTRACT

Page 21, lines 2-10 have been amended as follows:

A method for reordering a scan chain so that the meets given constraints are met and [[the]] minimizes peak power dissipation is minimized and disclosed. The given constraints include a maximum peak power dissipation, a maximum scan chain length and a maximum distance between two successive registers. The method includes embedding a developed tool can be embedded into [[the]] an existing VLSI design flow for low-power circuit designs. Furthermore, the characteristics [[are]] quickly judge judging if the problem has corresponding feasible solutions and searching the optimal solution. Modified data from the given Given the scan chain declaration data and the scan pattern data, the modified ones, which satisfy the constraints, can be obtained.